Novel 1T DRAM Cell for Low-Voltage Operation and Long Data Retention Time

Woojun LEE†, Kwangsoo KIM††, Nonmembers, and Woo Young CHOI†(a), Member

SUMMARY A novel one-transistor dynamic random access memory (1T DRAM) cell has been proposed for a low-voltage operation and longer data retention time. The proposed 1T DRAM cell has three features compared with a conventional 1T DRAM cell: low body doping concentration, a recessed gate structure, and a P+ poly-Si gate. Simulation results show that the proposed 1T DRAM cell has < 1-ns program time and > 100-ms data retention time under the condition of sub-1-V operating voltage.

key words: 1T DRAM, capacitorless DRAM, low voltage, data retention time

1. Introduction

Conventionally, the density of dynamic random access memory (DRAM) has been improved by scaling the cell size down. However, downscaling has faced physical limits recently. Therefore, for higher memory density, the one-transistor DRAM (1T DRAM) has been considered as one of the most promising candidates for next-generation memory [1]. A conventional DRAM cell needs one capacitor and one transistor for storing one bit of data. On the other hand, a 1T DRAM cell needs only one transistor for storing one-bit data. Thus, 1T DRAM cells feature simpler fabrication process and higher memory density than conventional DRAM cells. Also, the 1T DRAM cell is completely compatible with complementary metal-oxide-semiconductor (CMOS) process because it needs no capacitor.

For 1T DRAM cells, there have been three program methods: the MOS field-effect-transistor impact-ionization (MOSFET)-based method [2]–[4], gate-induced-drain-leakage (GIDL)-based method [5],[6], and bipolar-junction-transistor impact-ionization (BJT)-based method [7],[8]. Among them, the BJT-based method has the highest sensing current margin which leads to the longest data retention time. Thus, in this work, we have utilized the BJT-based method. However, as shown in Fig. 1(a), the BJT-based method requires higher drain voltage ($V_D$) than the MOSFET-based and the GIDL-based method. It means that the BJT-based method may be inappropriate for a low-voltage operation. As shown in Fig. 1(b), DRAM core voltages have been decreased from generation to generation and finally next-generation DRAM cells require sub-1-V operating voltage. In order to address this issue, in this paper, we have achieved a low-voltage BJT-based program by introducing a novel 1T DRAM cell. The performance of the proposed 1T DRAM cell has been evaluated by device simulation.

2. Simulation Results and Discussion

Figure 2 shows conventional and proposed 1T DRAM cell structure, respectively. The proposed 1T DRAM cell has three features compared with a conventional one: low body
111

![Diagram of conventional and proposed 1T DRAM cell structures.](image)

Fig. 2 Comparison between conventional and proposed 1T DRAM cell structures. Three ideas have been introduced to the proposed 1T DRAM cell: low $N_B$, a recessed gate structure, and a $P^+$ poly-Si gate.

doping concentration ($N_B$), a recessed gate structure, and a $P^+$ poly-Si gate. In order to solve the problem that the conventional 1T DRAM cells need high $V_D$ for high speed program, low $N_B$ has been introduced. However, low $N_B$ may increase drain disturbance. Thus, recessed gate structure has been used to suppress drain disturbance. Also, $P^+$ poly-Si gate electrode has been adopted to reduce the magnitude of operating gate voltage ($V_G$). The proposed 1T DRAM cell has short program time with low operating voltages thanks to those features. In order to compare the electrical characteristics of both kinds of DRAM cells, device simulation has been performed by using Silvaco ATLAS [9]. The Lombardi mobility model, the Shockley-Read-Hall (SRH) recombination model and the Selberherr’s impact ionization model have been used for simulation. Gate leakage current is ignored since gate oxide thickness ($t_{ox}$) is 3 nm and $V_G$ for 1T DRAM operation is less than 1 V. Also, poly depletion effect is ignored. In simulation, the conventional 1T DRAM cell has an $N_B$ of $10^{18}$ cm$^{-3}$ and an $N^+$ poly-Si gate while the proposed 1T DRAM cell has an $N_B$ of $1 \times 10^{15}$ cm$^{-3}$, and a $P^+$ poly-Si gate. Channel length ($L_{ch}$) and $t_{ox}$ have been fixed at 60 and 3 nm, respectively. Also, buried oxide thickness ($t_{BOX}$) and silicon-on-insulator thickness ($t_{SOI}$) have been fixed at 20 and 50 nm in both DRAM cells. Junction depth ($x_j$) of the proposed 1T DRAM cell is 30 nm.

Simulation results and features of the proposed 1T DRAM cell are shown in following section.

2.1 Low Body Doping Concentration

The proposed 1T DRAM cell adopts the BJT-based method [10] as a program method for high current sensing margin. Figure 3 shows the program operation mechanism of the 1T DRAM cell using the BJT-based method. Since reverse bias is applied to the drain junction of the 1T DRAM cell, in initial state, little amount of punch-through current flows between the source and drain as shown in Fig. 3(a): cut-
Fig. 4 (a) Electrical potential profiles following the A-A’ line shown in Fig. 3 in cut-off and active mode. A source-to-body potential barrier is lowered in active mode. (b) Total current density and (c) impact ionization rate of the 1T DRAM cell in cut-off mode and active mode.

Off mode. Hot electrons generate electron-hole pairs at the drain region. And generated holes are stored in the body of 1T DRAM cells. In that case, body potential increases and energy barrier between the source and body becomes lower, which turns on the BJT and increases electron injection from source. When current density increases, impact ionization rate at the drain region and hole concentration in the body increase abruptly: active mode. Figure 3(b) shows the punch-through current in the active mode [11]. Figure 4(a) shows electrical potential profiles following the A-A’ line shown in Fig. 3. In the cut-off mode, only punch-through current flows between the source and drain. However, when the operation of an intrinsic BJT changes from cut-off to active mode, the BJT current induced by a source-to-body barrier lowering dominates source-to-drain current ($I_D$). Therefore, when the intrinsic BJT changes from cut-off to active mode, $I_D$ and impact ionization rate increase abruptly as shown in Figs. 4(b) and (c). It should be noted that larger initial punch-through current makes the transition from cut-off to active mode more rapid. This is because more holes generated by large initial punch-through current lower the source-to-body energy barrier more rapidly. Figure 5(a) shows the transition of the intrinsic BJT states from cut-off to active mode as a function of $V_D$ and time. In the case of 1T DRAM cell with high $N_B$, high $V_D$ is needed to increase punch-through current. However, in the case of 1T DRAM cell with low $N_B$, large initial punch-through current is attained. Thus, the 1T DRAM cell with low $N_B$ can implement short program time in spite of low $V_D$. Program time is defined as the time when the abrupt transition occurs. Figure 5(b) shows the relationship between $N_B$ and program time. Even if low $V_D$ is applied, the 1T DRAM cells with low $N_B$ are able to achieve high speed program since program time decreases as $N_B$ decreases. Additionally, it is observed that program time is insensitive to $N_B$ in the case of low $N_B$. Therefore, low $N_B$ is desirable in terms of random dopant fluctuation (RDF) immunity.
2.2 Recessed Gate Structure

As mentioned above, low \( N_B \) is desirable for 1T DRAM applications. However, in the case of conventional 1T DRAM cells, it is difficult to lower \( N_B \) due to a severe short-channel effect. Hence, the proposed 1T DRAM cell utilizes the recessed gate structure to suppress the short-channel effect. Also, the recessed gate structure is beneficial in terms of array disturbance. Figure 6 shows the disturbance mechanisms in a memory array structure. Assuming that Cell 4 is in program mode with Cell 1, 2 and 3 in hold mode, high and low negative voltages are applied to Word Line 1 and 2, respectively. Bit Line 1 is grounded and high positive voltage is applied to Bit Line 2. In this case, unwanted cell disturbance may occur in Cell 2 and 3. Since Cell 2 and 3 are exposed to high positive \( V_D \) and small negative \( V_G \), respectively, drain and gate disturbances occur in the memory array. Since drain disturbance is generally severer than gate disturbance [12], only drain disturbance will be covered in this paper. The 1T DRAM cell with low \( N_B \) is more vulnerable to drain disturbance than one with high \( N_B \) in spite of its low-voltage and high-speed program operation. The proposed recessed gate structure can overcome this limitation. Figure 7 compares the immunity of the planar and recessed gate structure to drain disturbance. Figure 8 shows hole storage region of the planar and recessed gate structure. The SRH recombination is a critical factor considering the loss of stored holes which determines the cell state. It is known that the SRH recombination is proportional to the product of electron and hole concentration. In the case of the conventional 1T DRAM cell, as shown in Fig. 8(a), hole storage region is located adjacent to the source and drain region. Thus, high SRH recombination rate is inevitable, which limits data retention time significantly. However, in the case of the recessed gate structure, hole storage region is separated from the source and drain region. It means lower SRH recombination rate and longer data retention time than the conventional 1T DRAM cell. As shown in Fig. 9, the proposed 1T DRAM cell achieves 100-ms data retention time and high sensing current margin owing to the BJT-based method.

2.3 \( P^+ \) Poly-Si Gate

Finally, in order to adjust the operating voltages, the effect of gate work function on operating voltages is discussed. Figure 10 shows program time and punch-through current as a function of \( V_G \) in a \( P^+ \) and a \( N^+ \) poly-Si gate 1T DRAM cell with low \( N_B \) and recessed gate structure. Gate controllability degradation due to low \( N_B \) is compensated by the punch-through current suppression of the recessed gate structure. It means that the recessed gate structure is immune to drain disturbance. Also, Fig. 7 shows that recessed-gate 1T DRAM cells with low \( N_B \) are able to achieve high speed program in spite of low program efficiency.

Figure 8 shows hole storage region of the planar and recessed gate structure. The SRH recombination is a critical factor considering the loss of stored holes which determines the cell state. It is known that the SRH recombination is proportional to the product of electron and hole concentration. In the case of the conventional 1T DRAM cell, as shown in Fig. 8(a), hole storage region is located adjacent to the source and drain region. Thus, high SRH recombination rate is inevitable, which limits data retention time significantly. However, in the case of the recessed gate structure, hole storage region is separated from the source and drain region. It means lower SRH recombination rate and longer data retention time than the conventional 1T DRAM cell. As shown in Fig. 9, the proposed 1T DRAM cell achieves 100-ms data retention time and high sensing current margin owing to the BJT-based method.
Table 1 shows operation voltages for proposed 1T DRAM cell. Figure 11(a) shows $I_D$ of erased or programmed cell using operating conditions in Table 1 with 1- or 100-ms hold time. When $V_D$ and $V_G$ are 0.6 and 0 V, respectively, the ratio of $I_D$ of the programmed cell to $I_D$ of the erased cell ($R_{ID}$) is $\sim 250$ in spite of 100-ms hold time using cutoff and active mode state. It is smaller than that of other BJT-based 1T DRAM cells. However, $R_{ID}$ of $\sim 250$ is much higher than that of GIDL- or MOSFET-based 1T DRAM cells ($< 10$). Figure 11(b) represents operating voltage windows for the proposed 1T DRAM cell with the variation of the gate work function. Solid and dashed line box means the range of operating voltages for an N$^+$ and P$^+$ poly-Si gate, respectively. The operating voltages are determined to meet requirements: $< 1$-ns program time, $< 10$-ns erase time, $> 0.1$-ms drain disturbance program time and $> 100$-ms data retention time. It is observed that less than $-1$ V is needed to hold data in the case of N$^+$ poly-Si gate. If gate doping is changed from N$^+$ to P$^+$ to adjust gate work function, the range of the $V_G$ is shifted by 1.1 V. It means that sub-1-V high-speed operation is feasible in our proposed 1T DRAM cell and retention time is $\sim 100$ ms as shown in Fig. 9.

3. Conclusions

For a low-voltage and a high-speed operation of 1T DRAM cells, we have proposed a novel 1T DRAM cell which features low $N_B$, recessed gate structure and P$^+$ poly-Si gate. Low $N_B$ has been introduced for faster program operation. The recessed gate structure has been adopted to suppress a short-channel effect and array disturbance. P$^+$ poly-Si gate has been used for low-voltage operation. According to device simulation results, the proposed 1T DRAM cell shows faster programming with low operating voltages compared...
with a conventional 1T DRAM cell.

Acknowledgments

This work was supported in part by the National Research Foundation (NRF) of Korea funded by the Ministry of Education, Science and Technology (MEST) under Grants 2010-0019105 (Development of Future-Oriented Technology) and 2010-0027704 (Mid-Career Researcher Program) and in part by the Ministry of Knowledge Economy (MKE) of Korea under Grant NIPA-2010-C1090-1001-0003 (University ITRC support program supervised by the National IT Industry Promotion Agency) and in part by the Sogang University Research Grant of 2010.

References


Woojun Lee was born in Seoul, Korea, in 1984. He received the B.S. degree in Electronic Engineering from Sogang University, Seoul, Korea, in 2009. He is currently working toward the M.S. degree in electrical engineering in the Department of Electrical Engineering at the same university. His current research interests include CMOS and CMOS-compatible novel device modeling.

Kwangsoo Kim was born in Seoul, Korea, in 1958. He holds degrees from Sogang University (B.SEE, 1981, MSEEE, 1983 and PhD, 1992). From 1982 to 1998 he was with the Electronics and Telecommunications Research Institute (ETRI), working on silicon devices (CMOS, Bipolar & BiCMOS). From 1988 to 1992, he carried out his PhD dissertation at Sogang on the high speed and high density BiCMOS device. From 1999 to 2005 he was principal research engineer with IITA where he planned new component technology about Information & Communication Technology of Korea. From 2005 to 2008 he was principal research engineer with DGIST where he conducted research on IT convergence technology for intelligent vehicles. In 2008, he joined the Department of Sogang Institute of Advanced Technology at Sogang University, Seoul, Korea as an associate professor. His current research interests focus on the technology, modeling and reliability of MEMS sensors. Prof. Kim is also active in inventing the technology of energy harvest using piezo-electric materials.

Woo Young Choi was born in Incheon, Korea, in 1978. He received the B.S., M.S. and Ph.D. degrees in the School of Electrical Engineering from Seoul National University, Seoul, Korea in 2000, 2002 and 2006, respectively. From 2006 to 2008, he was with the Department of Electrical and Computer Sciences, University of California, Berkeley, USA as a post-doctor. In 2008, he joined the Department of Electronic Engineering, Sogang University, Seoul, Korea as an associate professor. He has authored or coauthored over 90 papers in international journals and conference proceedings and holds eight Korean patents. His current research interests include CMOS and CMOS-compatible novel device modeling, characterization, measurement, fabrication, and nano-electromechanical system (NEMS) technology. Prof. Choi received the Humantech Thesis Prize from Samsung Electronics in 2005 and also received the Doyeon Paper Award from Inter-university Semiconductor Research Center (ISRC), Seoul National University.